

EAST - [10727999.wsp:1]

File View Edit Tools Window Help

☐ Drafts
☐ Pending
☒ Active
☐ L1: (186179) MOS or metal near oxide near semiconductor or CMOS
☐ L2: (496) 1 and substrate and gate near dielectric and spacer and epitaxial and scribe and sour...
☐ L3: (489) 1 and substrate and gate near dielectric and spacer and epitaxial and scribe and sour...
☐ L4: (1) ("6812527").PN
☐ Failed
☐ Saved
☐ Favorites
☐ Tagged (0)
☐ UDC
☐ Queue
☐ Trash

Search:
 OR: US-PCFDP; USPAT; EPO- JPO ☐ Phrase
 Default grammar: OR ☐ Highlight all hit terms only

1 and substrate and gate near dielectric and spacer and epitaxial and scribe and source and drain and (dielectric insulat\$3) and (contact\$1 metal)

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050055494 A1	20050310	19	STRUCTURE AND METHOD FOR SILICIDED METAL GATE TRANSISTORS	711/103		
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20050054168 A1	20050310	12	Semiconductor structures employing strained material layers with defined impurity gradients and methods for fabrication same	438/300		
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20050051851 A1	20050310	15	STRUCTURE AND METHOD OF MAKING STRAINED CHANNEL CMOS TRANSISTORS HAVING LATTICE MISMATCHED EPITAXIAL EXTENSION AND METHOD TO PRODUCE TRANSISTOR HAVING REDUCED GATE HEIGHT	257/369	436/199	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20050048732 A1	20050303	13	METHOD TO PRODUCE TRANSISTOR HAVING REDUCED GATE HEIGHT	438/305		
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20050048703 A1	20050303	20	Method to control device threshold of SOI MOSFET's	438/149	438/164; 438/459	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20050045947 A1	20050303	14	THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS	257/336	257/213; 257/333	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20050040444 A1	20050224	20	Strained-channel fin field effect transistor (FET) with a uniform channel thickness and separate gates	257/288	257/392; 438/197; 438/275	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20050037582 A1	20050217	19	DEVICE THRESHOLD CONTROL OF FRONT-GATE SILICON-ON-INSULATOR MOSFET USING A SELF-ALIGNED BACK-GATE	438/281	438/296	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20050037558 A1	20050217	6	Method for fabricating transistor having fully silicided gate	438/197	438/300; 438/592	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20050035470 A1	20050217	19	Strained channel complementary field-effect transistors and methods of manufacture		257/900	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20050035455 A1	20050217	9	Device with low-k dielectric in close proximity thereto and its method of fabrication	257/758		